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(71)Applicant : **NEC CORP**
(72)Inventor : **ANDO MASATERU**

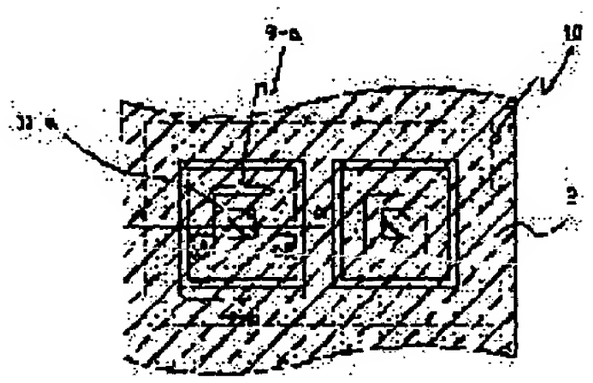
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

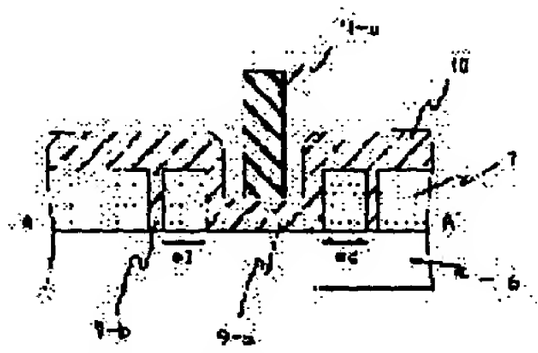
PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor device and this semiconductor device for improving the accuracy of the positioning of a lower layer pattern with an upper layer pattern in a photolithography process.

SOLUTION: A pair of box masks for measuring the relative positions of a lower layer pattern with upper layer pattern of a semiconductor device are provided in a box mark formation region. One box mark from among the pair of box marks is constituted of an opening groove 9-a formed on an inter-layer insulating film 7 and a rectangular slit 9-b having almost the same center as the opening groove 9-a, and the other box mark among the pair of box marks is a positioning mark 11-a formed on the opening groove. Thus, when reflow occurs again in the inter-layer insulating film 7, the shape change of the edge part of the opening groove 9-a can be reduced to a minimum.

(A)



(B)



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[Date of request for examination] 27.10.1998

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[Date of final disposal for application]

[Patent number]

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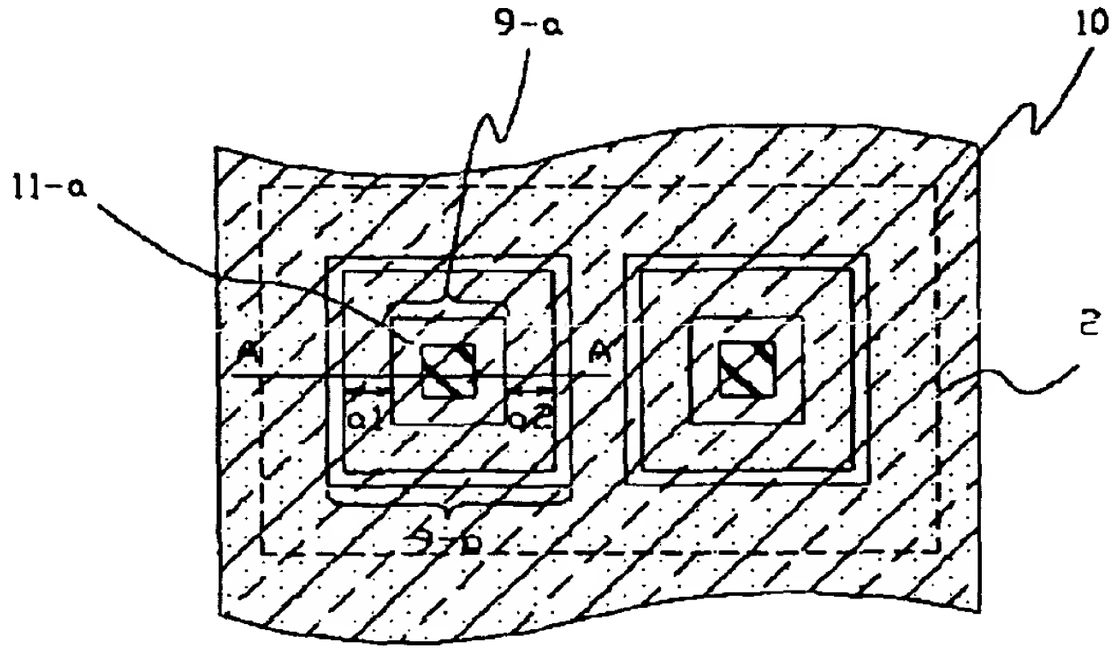
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

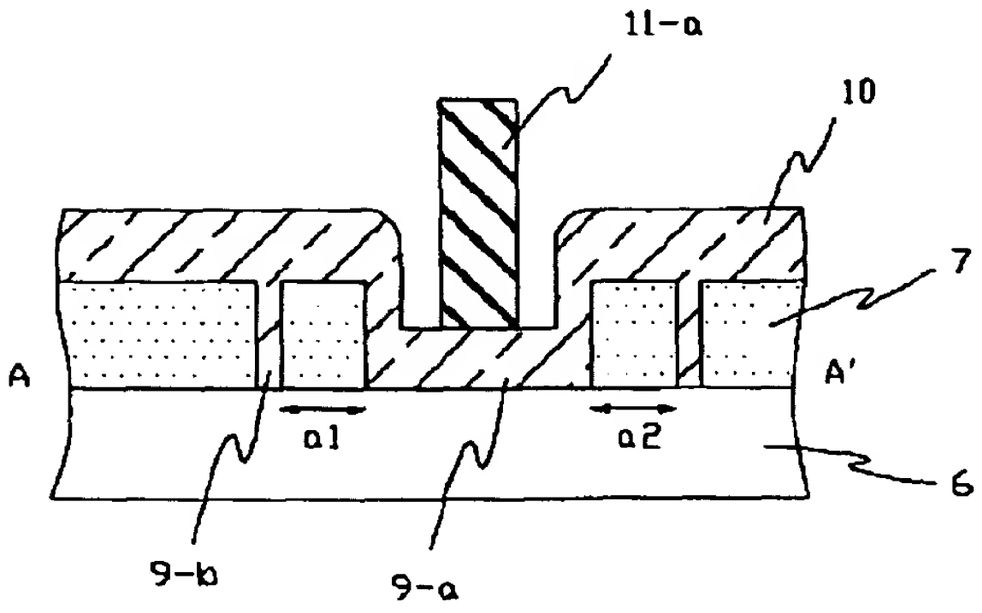
DRAWINGS

[Drawing 1]

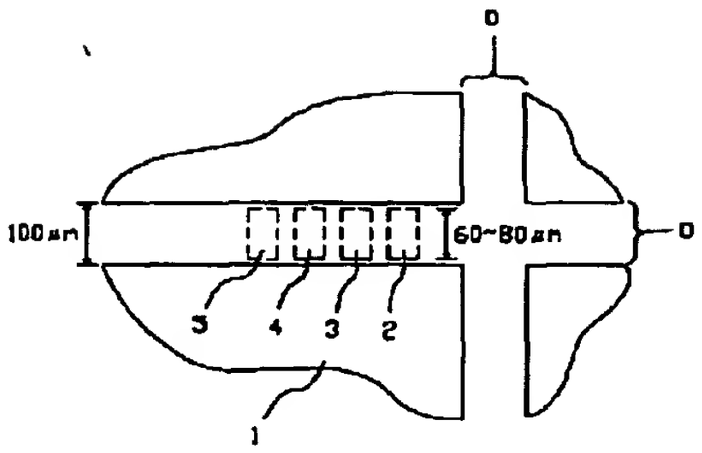
(A)



(B)

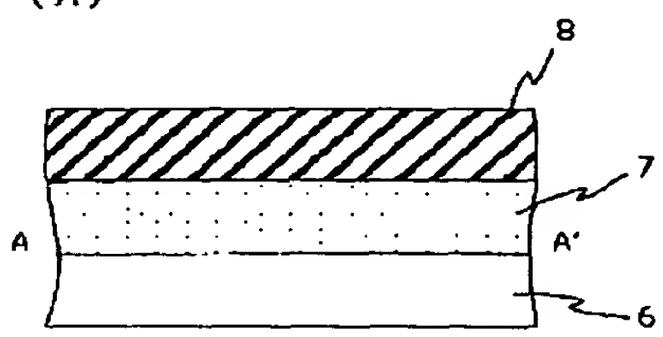


[Drawing 5]

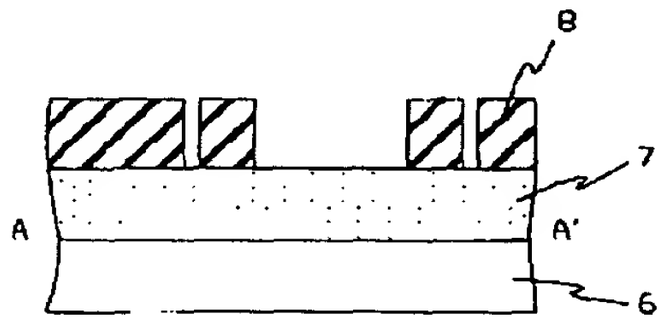


[Drawing 2]

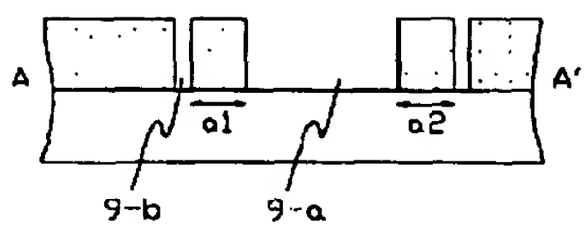
(A)



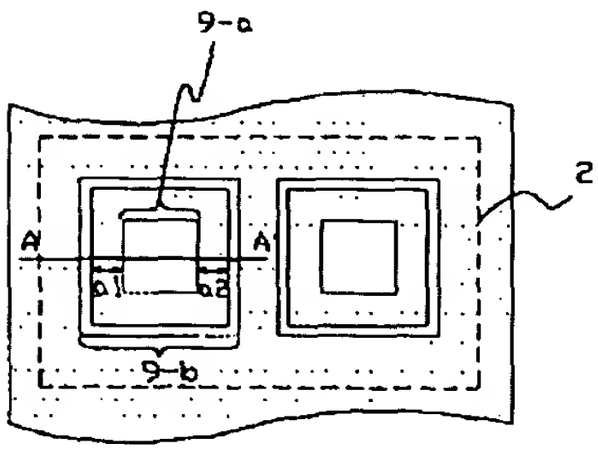
(B)



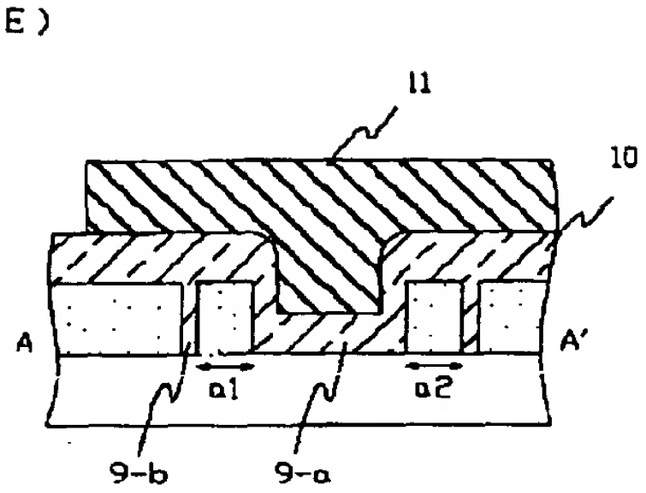
(C)



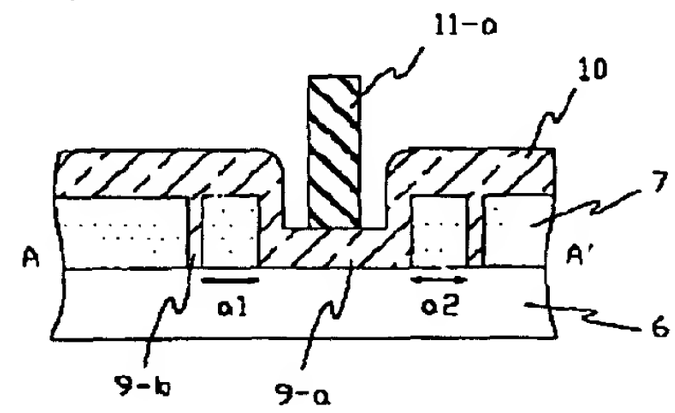
(D)



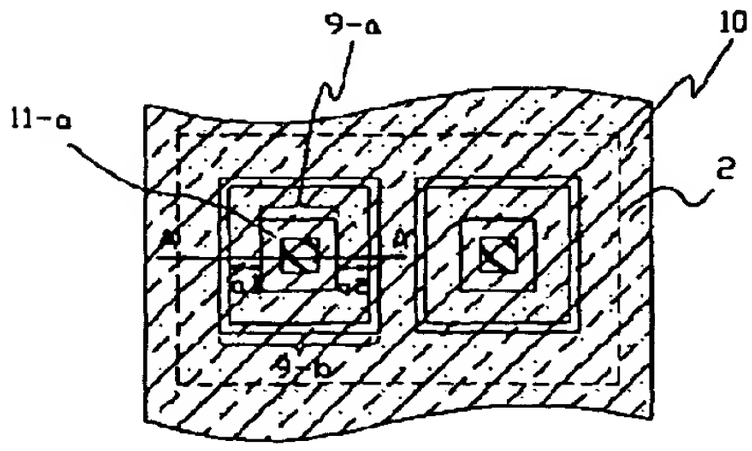
(E)



(F)

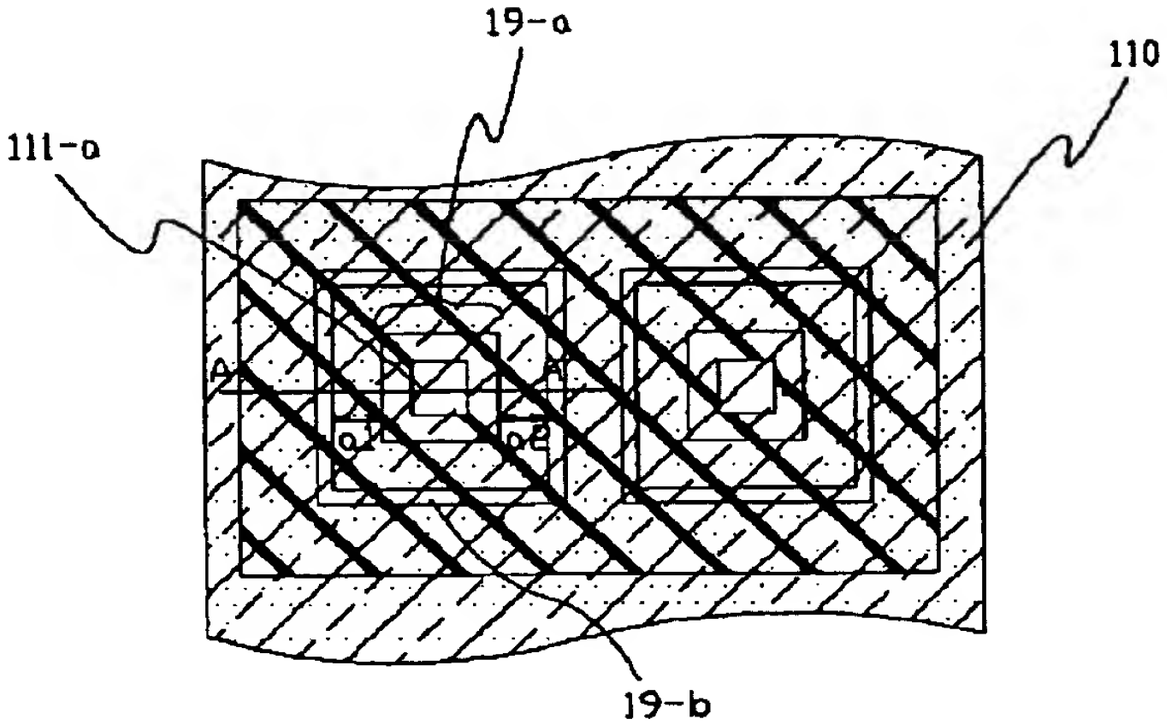


(G)

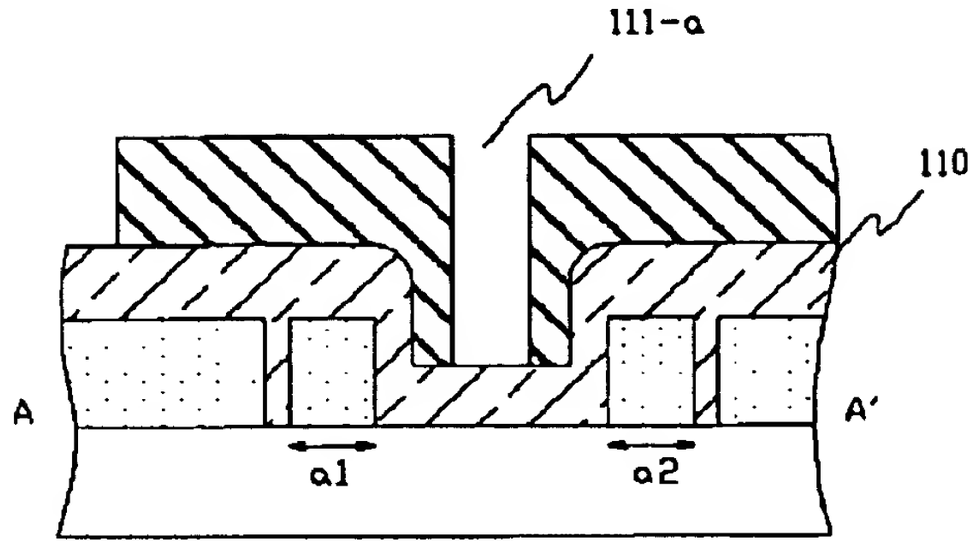


[Drawing 3]

(A)

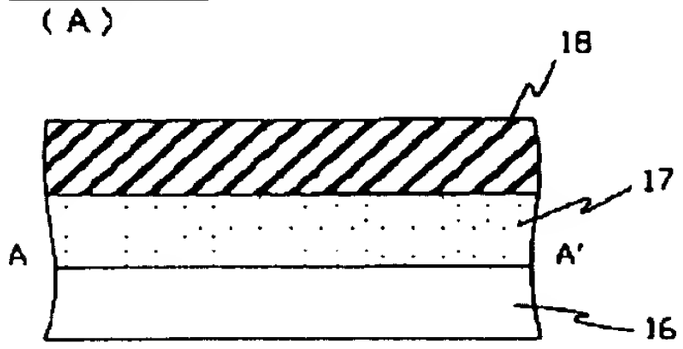


(B)

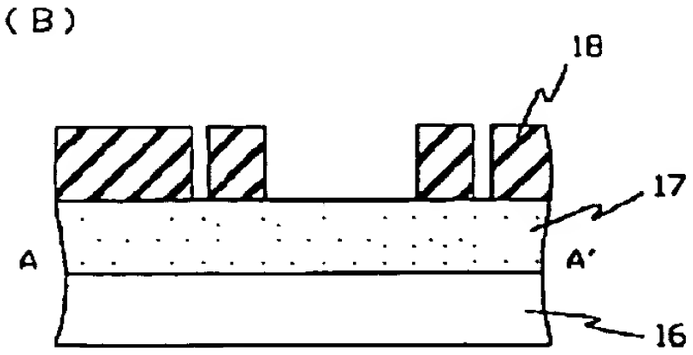


[Drawing 4]

(A)

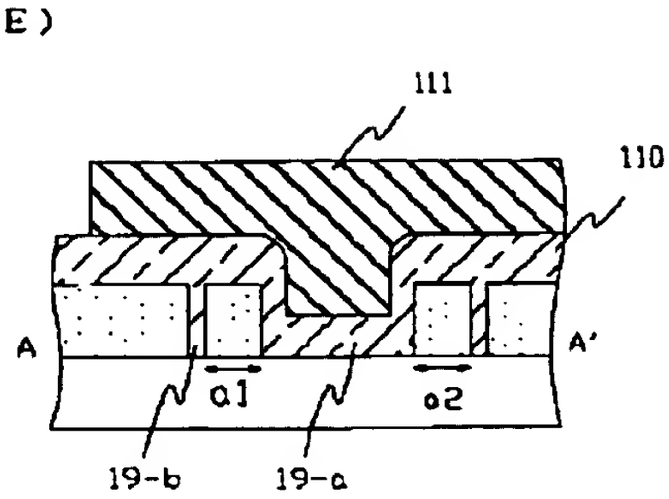


(B)

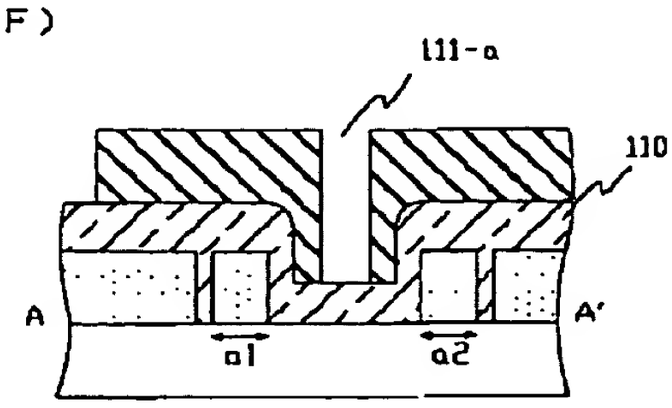


(C)

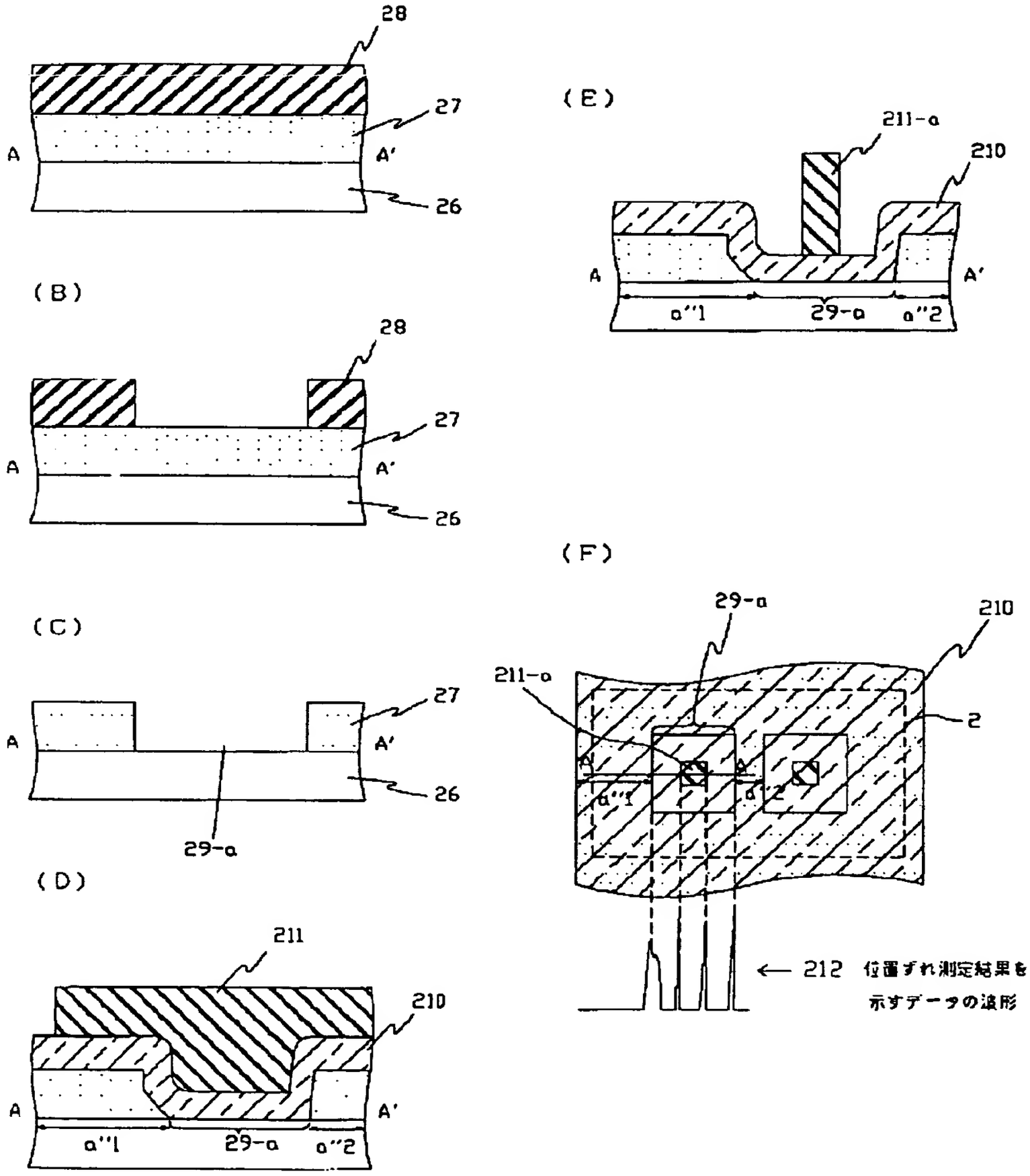
(E)



(F)



[Drawing 6]



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture technique of a semiconductor device and a semiconductor device. It is related with the manufacture technique of the semiconductor device and semiconductor device which can aim at enhancement in precision of position doubling for making the pattern and the design pattern of the following process which preexist on a semiconductor substrate the optimum relative-position relation in the phot lithography process of the manufacturing processes of a semiconductor device especially.
[0002]
[Description of the Prior Art] The development of the semiconductor device of super-high accumulation is furthered energetically in recent years, and in order to attain detailed-izing and high-density-izing of a semiconductor device in connection with it, the further enhancement in the position doubling precision of the mask in an indispensable phot lithography process has come to require it of formation of semiconductor device structure strongly.
[0003] Usually, in a manufacture of a semiconductor device, the laminating of the pattern formed on the semiconductor substrate by various material layers, such as a metal membrane, a semiconductor layer, and an insulating body membrane, is carried out one by one, and the semiconductor device of the fine structure is formed. In carrying out the laminating of the pattern for these semiconductor devices, in a phot lithography process, it is necessary to pile up and form the following upper pattern for the pattern of a lower layer formed at the last process.
[0004] In this phot lithography process, in case the phot lithography process of the upper pattern is performed, a mask pattern is piled up and used as the pattern of a lower layer by predetermined specification. The height of the position doubling precision at the time of piling up these patterns comes to require, and the technique for raising position doubling precision is searched for as a semiconductor device high-density[detailed-izing and]-izes.
[0005] Generally, this position doubling precision forms one pair of box marks in the lower layer pattern and the upper pattern of a semiconductor chip, and is computed by measuring a gap of the position during these box marks. For example, a gap (the amount of gaps of alignment) of the relative position of a lower layer pattern and the upper pattern is computed by measuring the relative position during one pair of box marks which consist of a certain mark currently formed on the semiconductor substrate, and a position doubling mark which consists of a photoresist obtained according to a phot lithography process, and computing a gap of the relative position between these. Based on the amount of gaps of this alignment, position doubling of a lower layer pattern and the upper pattern is performed.
[0006] For example, the manufacture technique of the semiconductor device and semiconductor device which compute the relative position with the photoresist layer which is the layer insulation layer and the upper pattern which are a lower layer pattern is indicated by measuring the relative position during one pair of box marks which consist of a position doubling mark which becomes JP,9-232221,A from the photoresist prepared on the thin film deposited the slot of the shape of a slit prepared in the predetermined field of a layer insulation layer, and on a layer insulation layer.
[0007] The box mark used on the other hand in order to detect position doubling precision is prepared in the field other than the field in which elements, such as a transistor, are formed. That is, as shown in drawing 5 , the box mark formation field 2-3-4-5 is formed not on the chip field (product field) 1 but on the scribe line 0. Thereby, the amount of gaps of alignment can be computed, without causing increase of chip area. Moreover, since one box mark formation field per 1 time of alignment is used, the box mark formation fields used for every alignment differ. For this reason, a box mark formation field is needed by the number of times which performs alignment at least.
[0008] Thus, when performing position doubling of a lower layer pattern and the upper pattern based on the amount of gaps of the alignment computed from the relative position gap during a box mark, the conspicuousness of **********-** is raised as one of the big elements which influence the precision of position doubling. The process which forms **********-** for position doubling in drawing 6 in the manufacture technique of the conventional semiconductor device and the conventional semiconductor device in the phot lithography process of the conductor material layers used as an electrode material into DRAM, such as a polycrystal silicon layer, is shown. Here, the case where the aforementioned box mark is formed in the box mark formation field 2 shown in drawing 5 as an example is explained. In the manufacture technique of the conventional semiconductor device and a semiconductor device, as shown in drawing 6 (A), the layer insulation layer 27 is formed on the semiconductor substrate 26. The layer insulation layers 27 are SiO2, a TEOSBPSG (Tetraethoxyorthosilicate Borophosphosilicate glass) layer, etc., and in a chip field (product field), in order to insulate mutually the word line (not shown) which consists of an element and the 1st polycrystal silicon layer, and the bit line (not shown) which consists of an element and the 2nd polycrystal silicon layer, they consist of a layer insulation layer more than two-layer at least. In addition, the thickness of the layer insulation layer 27 in this time is about about 1000nm. In the chip field (product field) 1, although the word line and bit line which consist of the 1st and 2nd polycrystal silicon layers are

formed, since elements, such as a transistor, are not formed in a **********-** formation field, a word line, a bit line, etc. which consist of the above 1st and the 2nd polycrystal silicon layer are not formed in the **********-** formation field 2. Next, as shown in drawing 6 (A), a photoresist 28 is applied the whole surface on the layer insulation layer 27.

[0009] Then, as shown in the drawing 6 (B) and the drawing 6 (C), it sets to the chip field (product field) 1 using conventional phot lithography technique and conventional etching technique. Opening slot 29-a is formed in the **********-** formation field 2 shown in drawing 5 as **********-** at the same time it forms the contact (not shown) for connecting the store electrode which consists of conductor material layers 210, such as a polycrystal silicon layer, on the aforementioned N-diffusion layer. Then, after forming the conductor material layer 210 with a thickness [used as a store electrode] of about about 500-700nm in the chip field (product field) 1 and the **********-** formation field 2, a photoresist 211 is given to the whole surface as shown in drawing 6 (D). Furthermore, as shown in drawing 6 (E), position doubling mark 211-a is formed using the phot lithography technique generally used on the conductor material layer 210 in the aforementioned opening slot 29-a. The plan corresponding to drawing 6 (E) is shown in drawing 6 (F). Generally, a gap of the relative position of position doubling mark 211-a and opening slot 29-a which are shown in drawing 6 (F) is mechanically computed by applying the existing image processing technique. The wave 212 which shows the data of the position gap measurement result of opening slot 29-a obtained from the existing image processing technique and position doubling mark 211-a is combined with opening slot 29-a and position doubling mark 211-a, and is shown in drawing 6 (F).

[0010]

[Problem(s) to be Solved by the Invention] However, there were the following troubles in the manufacture technique of the conventional semiconductor device and semiconductor device which are shown in drawing 6 . Two or more heat treatment processes are usually included in the manufacturing process of the conventional semiconductor device. As a typical thing in it, heat treatment of the layer insulation layer formed on the semiconductor substrate is mentioned. When forming some layer insulation layers (for example, SiO2, TEOSBPSG layer, etc.) on a semiconductor substrate, if the formed layer insulation layer remains as it is, it has [on a front face] irregularity and is not flat. Therefore, generally, in order to obtain sufficient flat nature in the manufacturing process of a semiconductor device, a flattening is carried out by heat-treating and carrying out a reflow (fluidization) to the aforementioned layer insulation layer. The flattening of the layer insulation layer is enough carried out by performing the aforementioned heat treatment above the predetermined temperature in which a layer insulation layer carries out a reflow (fluidization) in that case. Moreover, if the layer insulation layer which carried out a reflow at once is not temperature higher than the temperature (reflow temperature) when carrying out a reflow of the aforementioned layer insulation layer, not starting a reflow again is known.

[0011] There was little influence which it has on semiconductor devices, such as a device property, on the other hand even if a semiconductor device is not so detailed in the conventional semiconductor device, and the temperature of heat treatment aiming at the flattening of the aforementioned layer insulation layer is high a little, since the density was also low. However, when the temperature (reflow temperature) of heat treatment at the time of performing a flattening in connection with detailed-izing and high-density-izing of the latest semiconductor device was an elevated temperature, the influence affect semiconductor devices, such as a device property, became large as compared with the conventional semiconductor device. Therefore, since it needs to heat-treat at as low temperature as possible in the temperature requirement which can fully carry out the flattening of the layer insulation layer when performing heat treatment aiming at the flattening of a layer insulation layer, heat treatment at the time of performing a flattening has come to be performed at low reflow temperature as compared with the former. However, the problem that the direction of the temperature of heat treatment used at other processes other than the flattening of the aforementioned layer insulation layer will become high has arisen as a flattening comes to be performed at low reflow temperature in this way as compared with the former.

[0012] For example, it sets to the manufacture technique of the conventional semiconductor device and semiconductor device which are shown in drawing 6 . For example, after performing heat treatment aiming at the flattening of the layer insulation layer 27 which consists of SiO2, a TEOSBPSG layer, etc. at 800 degrees C (reflow temperature), Heat treatment aiming at an activation of the ion poured in by ion-implantation etc. (for example, under N2 ambient atmosphere) When 10 minutes is given in 850 degrees C, that the temperature (850 degrees C) of the heat treatment process aiming at an activation of the aforementioned ion etc. is higher than the reflow temperature (800 degrees C) of the layer insulation layer 27 by the cause The layer insulation layer 27 starts a reflow (re-fluidization) again, is missing from the base section near the base section of the lateral portion of opening slot 29-a, and the configuration of the layer insulation layer 27 deforms. The degree of configuration change of the edge fraction (fraction applied to the base section near the base section of the lateral portion of opening slot 29-a) of this opening slot 29-a is proportional to the volume of the layer insulation layer 27 contiguous to the outside of opening slot 29-a. Namely, since the volume of the layer insulation layer 27 with which it leaves as compared with the remnants width of face a"2 shown in drawing 6 (F), and leaves from a width-of-face a "remnants width-of-face asince 1 is larger"2 side, and the direction of width-of-face a"1 side adjoins is large, The edge fraction of opening slot 29-a by the side of the remnants width of face a"1 leaves, and compared with the edge fraction by the side of width-of-face a"2, the degree of configuration change will become large, and it will become a configuration which eats into the conductor material layer 210 formed behind. therefore -- a position -- doubling -- a mark -- 211 -- - -- a -- and -- opening -- a slot -- 29 -- - -- a -- it can set -- a position -- a gap -- an amount -- existing -- an image processing technique -- using -- having measured -- a case -- drawing -- six -- (-- F --) -- being shown -- as -- a position -- a gap -- measurement -- a result -- being shown -- data -- a wave -- 212 -- inside -- opening -- a slot -- remnants -- Since it became difficult to read correctly the amount of gaps of the relative position during a box mark (between position doubling mark 211-a and opening slot 29-a) as the result, the problem that the position doubling precision between a lower layer pattern and the upper pattern fell remarkably had arisen.

[0013] this invention is made in view of the problem in the above conventional technique. In the phot lithography process in the manufacturing process of a semiconductor device, in case the purpose of this invention performs position doubling between the design patterns of the following process which is the pattern and the upper pattern which preexist on the

semiconductor substrate which is a lower layer pattern, it is offering the manufacture technique of a semiconductor device and the semiconductor device which can aim at enhancement in the precision of the aforementioned position doubling.

[0014]

[Means for Solving the Problem] This 1st invention offered in order to solve the above subject is the manufacture technique of the semiconductor device characterized by to include the process which forms in an equidistant position mostly the slit of the configuration which encloses an opening slot from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least while it forms an opening slot in the predetermined field of the layer insulation layer formed on the semiconductor substrate.

[0015] While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate according to the manufacture technique of the semiconductor device invention of this application 1st which has the above-mentioned configuration By including the process which forms in an equidistant position mostly the slit of the configuration which encloses an opening slot from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least Since a layer insulation layer is arranged equally [****] between an opening slot and a slit, when a layer insulation layer starts a reflow again, configuration change of the edge fraction of an opening slot can be stopped to the minimum extent. Though configuration change of the edge fraction of an opening slot furthermore happens to some extent in this case Since the layer insulation layer is divided almost equally by the slit of the configuration which encloses the opening slot mostly installed in the equidistant position from the periphery of an opening slot to the center of an opening slot, From configuration change of the edge fraction of an opening slot becoming almost of the same grade to the center of an opening slot Since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown turns into almost symmetrical type to the center of an opening slot when position gap measurement is performed, the amount of position gaps can be detected correctly and position doubling precision is not reduced. Enhancement in position doubling precision can be aimed at by the above.

[0016] Moreover, it is characterized by the manufacture technique of the semiconductor device invention of this application 2nd including the process which forms the slit of the shape of a rectangle which has the same center mostly with an opening slot, and the process of an opening slot which forms a position doubling mark in part at least while it forms an opening slot in the predetermined field of the layer insulation layer formed on the semiconductor substrate.

[0017] While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate according to the manufacture technique of the semiconductor device invention of this application 2nd which has the above-mentioned configuration By including the process which forms the slit of the shape of a rectangle which has the same center mostly with an opening slot, and the process of an opening slot which forms a position doubling mark in part at least When the layer insulation layer arranged between an opening slot and a slit becomes equal [****] to the center of an opening slot and a layer insulation layer starts a reflow again, configuration change of the edge fraction of an opening slot can be suppressed to the minimum extent. Though the configuration of the edge fraction of an opening slot furthermore changes to some extent in this case Since the layer insulation layer arranged between an opening slot and a slit by dividing a layer insulation layer by the slit of the shape of a rectangle which has the same center mostly with an opening slot becomes almost equal to the center of an opening slot, From configuration change of the edge fraction of an opening slot occurring almost corresponding to the distance from the center of an opening slot When position gap measurement is performed, the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown becomes the thing corresponding to the distance from the center of an opening slot mostly, and can measure the amount of position gaps correctly from the data in which the aforementioned position gap measurement result is shown. Enhancement in position doubling precision can be aimed at by the above.

[0018] Moreover, it is characterized by the manufacture technique of the semiconductor device invention of this application 3rd including the process which forms a frame-like slit so that it may be mostly located in the equal distance from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least while it forms an opening slot in the predetermined field on the layer insulation layer formed on the semiconductor substrate.

[0019] While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate according to the manufacture technique of the semiconductor device invention of this application 3rd which has the above-mentioned configuration By including the process which forms a frame-like slit so that it may be mostly located in the equal distance from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least From the layer insulation layer between an opening slot and a slit being arranged equally [****] to the center of an opening slot, when a layer insulation layer starts a reflow again, configuration change of the edge fraction of an opening slot can be suppressed to the minimum extent. Though the configuration of the edge fraction of an opening slot furthermore changes to some extent in this case Since the layer insulation layer between an opening slot and a slit is arranged almost equally to the center of an opening slot by dividing a layer insulation layer by the slit of the shape of a frame arranged so that it may be mostly located in the equal distance from the periphery of an opening slot, The edge fraction of an opening slot from configuration change cutting almost corresponding to the distance from the center of an opening slot Since the wave of the data in which the position gap measurement result in the edge fraction of an opening slot is shown becomes the thing corresponding to the distance from the center of an opening slot mostly similarly, the amount of position gaps can be correctly measured from the data in which the aforementioned position gap measurement result is shown. Enhancement in position doubling precision can be aimed at by the above.

[0020] Moreover, the manufacture technique of the semiconductor device invention of this application 4th is the manufacture technique of the semiconductor device of either 1 of the invention of this application 1st - this application 3rd, and it is characterized by setting up the width of face of a position doubling mark smaller than the width of face of an opening slot.

[0021] Since a position doubling mark can be installed in the interior of an opening slot by setting up the width of face of a position doubling mark smaller than the width of face of an opening slot according to the manufacture technique of the

semiconductor device invention of this application 4th which has the above-mentioned configuration, in the position gap measurement using the existing image processing technique, the contrast of a position doubling mark fraction becomes clear, and it becomes easy to detect a position doubling mark. Thereby, since the amount of position gaps between an opening slot and a position doubling mark is correctly detectable, enhancement in position doubling precision can be aimed at.
[0022] Moreover, the manufacture technique of the semiconductor device invention of this application 5th is the manufacture technique of the semiconductor device of either 1 of the invention of this application 1st - this application 4th, and it is characterized by extracting a position doubling mark and forming as structure.
[0023] Although a position doubling mark extracts and forming as structure according to the manufacture technique of the semiconductor device invention of this application 5th which has the above-mentioned configuration, since it is correctly detectable in the amount of position gaps between an opening slot and a position doubling mark by choosing suitably whether it leaves a position doubling mark and it considers as structure, or it extracts and it considers as structure, and using it according to the specification of a product, the enhancement in position doubling precision can plan.
[0024] Moreover, one pair of box marks for measuring the relative position of the lower layer pattern of a semiconductor device and the upper pattern set this 6th invention to the semiconductor device which it comes to prepare in a box mark formation field. The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks, It consists of a slit of the configuration which encloses the opening slot mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side is the semiconductor device characterized by being the position doubling mark formed in opening Mizogami among one pair of box marks.
[0025] It is prepared in the field in which the **********-** formation field said to this application is a field in which **********-** is formed, and the element on a semiconductor device is not formed. The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks according to the semiconductor device of invention of this application 6th which has the above-mentioned configuration, By being the position doubling mark to which it consisted of a slit of the configuration which encloses the opening slot mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since a layer insulation layer is arranged equally [****] and constituted between an opening slot and a slit, when a reflow occurs in a layer insulation layer again, it can obtain as a semiconductor device which has the opening slot which stopped configuration change of an edge fraction to the minimum extent. Though configuration change of the edge fraction of an opening slot furthermore happens to some extent in this case By coming to have the layer insulation layer divided from the periphery of an opening slot almost equally to the center of an opening slot by the slit of the configuration which encloses the opening slot arranged mostly in an equidistant position Since configuration change of the edge fraction of an opening slot becomes almost of the same grade to the center of an opening slot, When position gap measurement is performed, since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown turns into almost symmetrical type to the center of an opening slot, the amount of position gaps can detect correctly and does not reduce position doubling precision. It can obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate by the above, and the product yield is constituted as a good semiconductor device, and since it is possible to produce by the low cost in itself as a result, it can obtain cheaply.
[0026] Moreover, one pair of box marks for measuring the relative position of the lower layer pattern of a semiconductor device and the upper pattern set this 7th invention to the semiconductor device which it comes to prepare in a box mark formation field. The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks, It consists of a slit of the shape of a rectangle which has the same center mostly with an opening slot, and the box mark of another side is the semiconductor device characterized by being the position doubling mark formed in opening Mizogami among one pair of box marks.
[0027] It is prepared in the field in which the **********-** formation field said to this application is a field in which **********-** is formed, and the element on a semiconductor device is not formed. The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks according to the semiconductor device of invention of this application 7th which has the above-mentioned configuration, By being the position doubling mark to which it consisted of a slit of the shape of a rectangle which has the same center mostly with an opening slot, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since it comes to have the layer insulation layer arranged equally [****] between an opening slot and a slit, when a reflow occurs in a layer insulation layer again, it can obtain as a semiconductor device with which the opening slot where configuration change of an edge fraction was suppressed to the minimum extent was prepared. Even if the configuration of the edge fraction of an opening slot may furthermore change to some extent in this case Since configuration change of the edge fraction of an opening slot becomes of the same grade to the center of an opening slot by forming the layer insulation layer divided almost equally to the center of an opening slot by the slit of the shape of a rectangle which has the same center mostly with an opening slot, Since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown serves as an almost symmetrical configuration to the center of an opening slot similarly when position gap measurement is performed, the amount of position gaps can detect correctly and can maintain position doubling precision. It can obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate, the product yield is constituted as a good semiconductor device by the above, and it can obtain from the production by the low cost being possible as a result as a cheap semiconductor device.
[0028] Moreover, one pair of box marks for measuring the relative position of the lower layer pattern of a semiconductor

device and the upper pattern set invention of this octavus to the semiconductor device which it comes to prepare in a box mark formation field. The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks, It consists of a slit of the shape of a frame mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side is the semiconductor device characterized by being the position doubling mark formed in opening Mizogami among one pair of box marks.

[0029] The opening slot where it comes to form the box mark of the method of one in the predetermined field of the layer insulation layer formed on the semiconductor substrate among one pair of box marks according to the semiconductor device of invention of this octavus which has the above-mentioned configuration, By being the position doubling mark to which it consisted of a slit of the shape of a frame mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since the layer insulation layer arranged equally [****] is prepared between the opening slot and the slit, when a reflow occurs in the aforementioned layer insulation layer again, configuration change of an edge fraction can obtain as a semiconductor device which comes to have the opening slot suppressed to the minimum extent. Though configuration change of an edge fraction furthermore happens to an opening slot to some extent in this case Since a layer insulation layer is arranged almost equally to the center of an opening slot between an opening slot and an edge fraction by dividing the layer insulation layer by the slit of the shape of a frame mostly arranged from the periphery of an opening slot in an equidistant position, Since configuration change of the edge fraction of an opening slot happens almost corresponding to the distance from the center of an opening slot and the wave of the data in which the position gap measurement result in the edge fraction of an opening slot is shown turns into the wave corresponding to the distance from the center of an opening slot mostly similarly, The amount of position gaps can be correctly measured from the data in which the aforementioned position gap measurement result is shown. Since the production by the low cost is attained in itself as a result of being able to obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate and the product yield's is constituted as a good semiconductor device by the above, it can obtain as a cheap semiconductor device.

[0030]

[Embodiments of the Invention] Although the manufacture technique of a semiconductor device and the semiconductor device concerning the gestalt of 1 operation of this invention are hereafter explained with reference to drawing, the gestalt of the following operations is the manufacture technique of the semiconductor device concerning the gestalt of 1 operation of this invention, and only an example of a semiconductor device.

(1st operation gestalt) The manufacture technique of a semiconductor device and the semiconductor device concerning the gestalt of 1 operation of this invention are explained in detail with reference to drawing 1 , drawing 2 , and the drawing 5 . Drawing 5 is a plan showing the **********-** formation field given to the semiconductor device concerning the gestalt of 1 operation of this invention. In drawing 5 , the **********-** formation field 2-3-4-5 of 60-80 micrometers of ****s is installed on the scribe line 0 which is 100 micrometers of ****s which are the field in which the element on a semiconductor device 1 is not formed. The width of face of the scribe line 0 and a **********-** formation field is not limited to this. These **********-** formation fields are used only in one patterning per field, respectively. Therefore, a **********-** formation field is prepared by the number of times of patterning at least. In the gestalt of this operation, the box mark installed in the **********-** formation field 2 is explained as an example. In addition, in drawing 5 , although two **********-**s are formed in one **********-** formation field, the number of the box marks formed in one **********-** formation field is not limited to this. Drawing 1 (A) is drawing showing one pair of box marks installed in the **********-** formation field 2 of the semiconductor device concerning the gestalt of this operation. Drawing 1 (B) is a cross section in A-A' of the semiconductor device shown in drawing 1 (A). Drawing 2 (A) - view 2 (G) is drawing having shown in order the manufacturing process of **********-** in the phot lithography process of the conductor material layer 10 used as an electrode material of the aforementioned DRAM, when the semiconductor device concerning the gestalt of this operation is applied to DRAM.

[0031] Next, the semiconductor device concerning the gestalt of this operation is explained in detail. As shown in drawing 1 , one pair of two box marks are installed in the **********-** formation field 2 established in the semiconductor device concerning the gestalt of this operation. The one aforementioned pair of box marks are prepared in order to measure the relative position of opening slot 9-a prepared on the substrate of the semiconductor device which is a lower layer pattern, and position doubling mark 11-a which consists of a photoresist layer prepared on the conductor material layer 10 which is the upper pattern. The aforementioned box marks are one pair of box marks. among one pair of box marks the box mark of the method of one It consists of opening slot 9-a and the slit 9-b of the shape (configuration which encloses opening slot 9-a) of a frame mostly arranged from the periphery of opening slot 9-a in an equidistant position. The box mark of another side is position doubling mark 11-a formed on the conductor material layer 10 in opening slot 9-a among one pair of box marks. By using the one aforementioned pair of box marks, the relative position of opening slot 9-a prepared on the substrate of the semiconductor device which is a lower layer pattern, and position doubling mark 11-a which consists of the aforementioned photoresist layer prepared on the aforementioned conductor material layer 10 which is the upper pattern can be measured with a sufficient precision.

[0032] Next, the manufacture technique of the semiconductor device concerning the gestalt of this operation is explained in detail. In the manufacturing process of the semiconductor device concerning the gestalt of this operation, as shown in drawing 2 (A), the layer insulation layer 7 is formed on the semiconductor substrate 6 which consists of P type silicon etc. It is SiO2, TEOSBPSG layer, etc., and the layer insulation layer 7 forms the contact for connecting the store electrode which consists of conductor material layers 10, such as the 3rd polycrystal silicon layer, in the chip field (product field) 1 (shown in drawing 5), and N-diffusion layer, after forming the layer insulation layer 7 on the semiconductor substrate 6. Moreover, in

order that the layer insulation layer 7 may insulate mutually the word line (not shown) which consists of an element and the 1st polycrystal silicon layer, and the bit line (not shown) which consists of an element and the 2nd polycrystal silicon layer in the chip field (product field) 1, it consists of a layer insulation layer more than two-layer at least, and the thickness of the layer insulation layer 7 in this time is about 1000nm. In the chip field (product field) 1, although the word line and bit line which consist of the 1st and 2nd polycrystal silicon layers are formed, since elements, such as a transistor, are not formed in the **********-** formation field 2, a word line, a bit line, etc. which consist of the 1st and 2nd polycrystal silicon layers are not formed in the **********-** formation field 2. Next, a photoresist 8 is applied to the top of the layer insulation layer 7 as shown in drawing 2 (A).

[0033] Next, as shown in the drawing 2 (B) and the drawing 2 (C), the phot lithography technique and etching technique which are generally used are used. At the same time it forms the contact (not shown) for connecting the store electrode which consists of a conductor material layer 10 on the aforementioned N-diffusion layer in the chip field (product field) 1 Opening slot 9-a and slit 9-b which are the box mark of the method of one among one pair of box marks are formed in the box mark formation field 2. Moreover, as shown in drawing 2 (C), slit 9-b is formed so that the distance to four sides which constitute slit 9-b from four sides which constitute the aforementioned opening slot 9-a may become almost equal. For example, slit 9-b is formed in the shape of [of about 1 micrometer of ****s] a frame, and prepares slit 9-b in the configuration which encloses the periphery of the aforementioned opening slot 9-a so that the remnants width of face a1 and a2 may be about 10 micrometers. The plan corresponding to drawing 2 (C) is shown in drawing 2 (D). By the above configuration, the remnants width of face a1 and a2 on the layer insulation layer 7 which adjoins opening slot 9-a becomes the almost same length by dividing the layer insulation layer 7 by slit 9-b. Heat treatment aiming at an activation of the ion poured in by ion-implantation after the process shown above etc. (for example, it sets at 850 degrees C under N2 ambient atmosphere, and is heat treatment for about 10 minutes) A grade is given. When the temperature of heat treatment aiming at the aforementioned activation etc. is higher than the reflow temperature (temperature of heat treatment at the time of performing the flattening of the layer insulation layer 7) of the layer insulation layer 7 in the manufacture technique of the conventional semiconductor device and a semiconductor device, the layer insulation layer 7 starts a reflow again. As the result, since the configuration of the edge fraction (fraction applied to the base section near the base section of the lateral portion of opening slot 9-a) of opening slot 9-a changes remarkably, position doubling precision falls by the contrast of the edge fraction of opening slot 9-a becoming not clear. However, it sets to the semiconductor device concerning the gestalt of this operation. By using one pair of **********-**s The material layer which the configuration of the edge fraction (fraction applied to the base section near the base section of the lateral portion of opening slot 9-a) of opening slot 9-a changes, and was prepared on opening slot 9-a even when a reflow with the layer insulation layer 7 for the second time was started (in the gestalt of this operation) Since aggravation of a configuration to which the layer insulation layer 7 eats into the ******** material layer 10 can be prevented, it is easily avoidable that position doubling precision falls by the contrast of the edge fraction of opening slot 9-a becoming not clear. In the manufacture technique of the conventional semiconductor device and a semiconductor device, the condition of configuration change of the edge fraction of opening slot 9-a is proportional to the volume of the layer insulation layer 7 contiguous to the outside of opening slot 9-a, and the influence by the reflow of the layer insulation layer 7 for the second time becomes large so that the volume of the adjoining layer insulation layer 7 is large. By therefore, the thing for which the remnants width of face a1 and a2 of the layer insulation layer 7 which adjoins opening slot 9-a is reduced to the grade which divides the layer insulation layer 7 in slit 9-b, and does not have trouble at the time of position gap measurement Since a configuration and **** to which the layer insulation layer 7 eats into the material layer (it sets in the gestalt of this operation and is the conductor material layer 10) which the configuration of the edge fraction of opening slot 9-a changes, and was prepared on opening slot 9-a can be prevented easily, A fall of the contrast of the edge fraction of opening slot 9-a at the time of the position gap measurement during a box mark can be prevented. Though configuration change of the edge fraction of opening slot 9-a furthermore happens to some extent in this case, since the layer insulation layer 7 is divided almost equally by slit 9-b to the center of opening slot 9-b, From configuration change of the edge fraction of opening slot 9-b becoming of the same grade to the center of opening slot 9-a Similarly, since the same type is acquired to the center of opening slot 9-a, the wave of the data in which the position gap measurement result in the edge fraction of opening slot 9-a is shown does not cause a fall of position doubling precision. Enhancement in position doubling precision can be aimed at by the above.

[0034] Next, as shown in drawing 2 (E), after forming the conductor material layer 10 which consists of the 3rd polycrystal silicon layer with a thickness [which serves as a store electrode (not shown) in the chip field (product field) 1] of about 500-700nm etc., a photoresist 11 is given to the whole surface as shown in drawing 2 (E). Furthermore, using the phot lithography technique generally used, as shown in drawing 2 (F), position doubling mark 11-a which is the box mark of another side among one pair of box marks is formed on the conductor material layer 10 in opening slot 9-a. The plan corresponding to drawing 2 (F) is shown in drawing 2 (G). Generally, as shown in drawing 2 (G), the relative position of the lower layer pattern prepared on the substrate of a semiconductor device and the upper pattern prepared on the lower layer pattern can be measured by computing mechanically the relative amount of position gaps of position doubling mark 11-a and opening slot 9-a which consist of a photoresist with the application of the existing image processing technique.

[0035] (2nd operation gestalt) The manufacture technique of a semiconductor device and the semiconductor device which are again applied to the gestalt of another operation of this invention are explained with reference to the drawing 3 and the drawing 4 . Drawing 3 (A) is drawing showing one pair of box marks installed in the **********-** formation field 2 of the semiconductor device concerning the 2nd operation gestalt of this invention. Drawing 3 (B) is a cross section in A-A' of the semiconductor device shown in drawing 3 (A). Drawing 4 (A) - view 4 (G) is drawing having shown in order the manufacturing process of **********-** in the phot lithography process of the conductor material layer 110 which consists of the 3rd polycrystal silicon layer used as an electrode material of the aforementioned DRAM, when the semiconductor device concerning the 2nd operation gestalt of this invention is applied to DRAM.

[0036] The manufacture technique of the semiconductor device and semiconductor device concerning the gestalt of operation of the 2nd of this invention shown in the drawing 3 and the drawing 4 The process (process shown in drawing 4 (A) - view 4 (E)) which gives the conductor material layer and photoresist which consist of the 3rd polycrystal silicon layer with a thickness [which serves as a store electrode in the chip field (product field) 1] of about 500-700nm etc. to the whole surface Since it is almost the same as that of the manufacturing process (refer to drawing 2 (A) - view 2 (E)) of the semiconductor device concerning the gestalt of operation of the 1st of this invention mentioned above, a detailed explanation is omitted. In the semiconductor device concerning the gestalt of this operation, as shown in drawing 3 Although the point which consists of opening slot 19-a and slit 19-b which it comes to form in the predetermined field of the layer insulation layer 17 with which the box mark of the method of one was formed on the semiconductor substrate among one pair of box marks is the same as the gestalt of operation of the 1st of this invention The points which are not the position doubling mark that leaves like the semiconductor device which requires the box mark of another side for the gestalt of operation of the 1st of this invention, and has structure but position doubling mark 111-a which inverts and extracts a mask data and is formed as structure among one pair of box marks differ. In the manufacture technique of the semiconductor device concerning the gestalt of this operation, as shown in drawing 4 (F), position doubling mark 111-a is formed on the conductor material layer 110 in opening slot 19-a using the existing phot lithography technique. In this case, unlike the position doubling mark which has the remnants structure installed in the semiconductor device concerning the gestalt of operation of the 1st of this invention mentioned above, the aforementioned position doubling mark 111-a inverts and extracts a mask data, and is formed with structure. Moreover, the plan corresponding to the cross section shown in drawing 4 (F) is shown in drawing 4 (G). When detecting a gap of lengthwise although the position gap of longitudinal direction (A-A' cross section) is detected by the semiconductor device and the semiconductor manufacture technique concerning the gestalt of this operation as shown in drawing 4 (G), it can apply easily. Furthermore, in the manufacture technique of the semiconductor device and semiconductor device concerning the gestalt of this operation, although the manufacturing process of **********-** in a phot lithography process and **********-** of the conductor material layers used as an electrode material of DRAM, such as a polycrystal silicon layer, was shown, it cannot be overemphasized that the semiconductor device and the semiconductor manufacture technique concerning the gestalt of this operation are applicable to other lithography process, other semiconductor devices, and semiconductor manufacturing processes.

[0037]

[Effect of the Invention] As mentioned above, the manufacture technique of the semiconductor device concerning this invention While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate By including the process which forms in an equidistant position mostly the slit of the configuration which encloses an opening slot from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least By reducing to the grade which does not have trouble at the time of position gap measurement, and installing the remnants width of face of the layer insulation layer between an opening slot and a slit Since the aforementioned layer insulation layer is arranged equally [****] around an opening slot, when a layer insulation layer starts a reflow again, configuration change of the edge fraction of an opening slot can be stopped to the minimum extent. Though configuration change of the edge fraction of an opening slot furthermore happens to some extent in this case Since the layer insulation layer is divided almost equally by the slit of the configuration which encloses the opening slot mostly installed in the equidistant position from the periphery of an opening slot to the center of an opening slot, From configuration change of the edge fraction of an opening slot becoming almost of the same grade to the center of an opening slot Since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown turns into almost symmetrical type to the center of an opening slot when position gap measurement is performed, the amount of position gaps can be detected correctly and position doubling precision is not reduced. Enhancement in position doubling precision can be aimed at by the above.

[0038] Moreover, the manufacture technique of the semiconductor device concerning this invention While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate By including the process which forms the slit of the shape of a rectangle which has the same center mostly with an opening slot, and the process of an opening slot which forms a position doubling mark in part at least By reducing to the grade which does not have trouble at the time of position gap measurement, and installing the remnants width of face of the layer insulation layer arranged between an opening slot and a slit Since the layer insulation layer arranged between an opening slot and a slit becomes equal [****] to the center of an opening slot, when a layer insulation layer starts a reflow again, configuration change of the edge fraction of an opening slot can be suppressed to the minimum extent. Though the configuration of the edge fraction of an opening slot furthermore changes to some extent in this case Since the layer insulation layer arranged between an opening slot and a slit by dividing a layer insulation layer by the slit of the shape of a rectangle which has the same center mostly with an opening slot becomes almost equal to the center of an opening slot, From configuration change of the edge fraction of an opening slot occurring almost corresponding to the distance from the center of an opening slot When position gap measurement is performed, the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown becomes the thing corresponding to the distance from the center of an opening slot mostly, and can measure the amount of position gaps correctly from the data in which the aforementioned position gap measurement result is shown. Enhancement in position doubling precision can be aimed at by the above.

[0039] Moreover, the manufacture technique of the semiconductor device concerning this invention While an opening slot is formed in the predetermined field of the layer insulation layer formed on the semiconductor substrate By including the process which forms a frame-like slit so that it may be mostly located in the equal distance from the periphery of an opening slot, and the process of an opening slot which forms a position doubling mark in part at least By reducing to the grade which does not have trouble at the time of position gap measurement, and installing the remnants width of face of the layer

insulation layer between an opening slot and a slit Since the aforementioned layer insulation layer between an opening slot and a slit is arranged equally [****] to the center of an opening slot, when a layer insulation layer starts a reflow again, cónfiguration change of the edge fraction of an opening slot can be suppressed to the minimum extent. Though the configuration of the edge fraction of an opening slot furthermore changes to some extent in this case Since the layer insulation layer between an opening slot and a slit is arranged almost equally to the center of an opening slot by dividing a layer insulation layer by the slit of the shape of a frame arranged so that it may be mostly located in the equal distance from the periphery of an opening slot, The edge fraction of an opening slot from configuration change cutting almost corresponding to the distance from the center of an opening slot Since the wave of the data in which the position gap measurement result in the edge fraction of an opening slot is shown becomes the thing corresponding to the distance from the center of an opening slot mostly similarly, the amount of position gaps can be correctly measured from the data in which the aforementioned position gap measurement result is shown. Enhancement in position doubling precision can be aimed at by the above.

[0040] Moreover, one pair of box marks for the semiconductor device concerning this invention measuring the relative position of the lower layer pattern of a semiconductor device and the upper pattern The opening slot which it comes to form in the predetermined field of the layer insulation layer with which it came to be prepared in a box mark formation field, and the box mark of the method of one was formed on the semiconductor substrate among one pair of box marks, By being the position doubling mark to which it consisted of a slit of the configuration which encloses the opening slot mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since a layer insulation layer is arranged equally [****] and constituted between an opening slot and a slit, when a reflow occurs in a layer insulation layer again, it can obtain as a semiconductor device which has the opening slot which stopped configuration change of an edge fraction to the minimum extent. Though configuration change of the edge fraction of an opening slot furthermore happens to some extent in this case By coming to have the layer insulation layer divided from the periphery of an opening slot almost equally to the center of an opening slot by the slit of the configuration which encloses the opening slot arranged mostly in an equidistant position Since configuration change of the edge fraction of an opening slot becomes almost of the same grade to the center of an opening slot, When position gap measurement is performed, since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown turns into almost symmetrical type to the center of an opening slot, the amount of position gaps can detect correctly and does not reduce position doubling precision. It can obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate by the above, therefore the product yield is constituted as a good semiconductor device, and since it is possible to produce by the the very thing low cost as a result, it can obtain cheaply.

[0041] Moreover, one pair of box marks for the semiconductor device concerning this invention measuring the relative position of the lower layer pattern of a semiconductor device and the upper pattern The opening slot which it comes to form in the predetermined field of the layer insulation layer with which it came to be prepared in a box mark formation field, and the box mark of the method of one was formed on the semiconductor substrate among one pair of box marks, By being the position doubling mark to which it consisted of a slit of the shape of a rectangle which has the same center mostly with an opening slot, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since it comes to have the layer insulation layer arranged equally [****] between an opening slot and a slit, when a reflow occurs in a layer insulation layer again, it can obtain as a semiconductor device with which the opening slot where configuration change of an edge fraction was suppressed to the minimum extent was prepared. Even if the configuration of the edge fraction of an opening slot may furthermore change to some extent in this case Since configuration change of the edge fraction of an opening slot becomes of the same grade to the center of an opening slot by forming the layer insulation layer divided almost equally to the center of an opening slot by the slit of the shape of a rectangle which has the same center mostly with an opening slot, Since the wave of the data in which the position gap measurement result in the edge fraction of the opening slot obtained by the aforementioned measurement is shown serves as an almost symmetrical configuration to the center of an opening slot similarly when position gap measurement is performed, the amount of position gaps can detect correctly and can maintain position doubling precision. It can obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate by the above, therefore the product yield is constituted as a good semiconductor device, and it can obtain from the production by the low cost being possible as a result as a cheap semiconductor device.

[0042] Moreover, one pair of box marks for the semiconductor device concerning this invention measuring the relative position of the lower layer pattern of a semiconductor device and the upper pattern The opening slot which it comes to form in the predetermined field of the layer insulation layer with which it came to be prepared in a box mark formation field, and the box mark of the method of one was formed on the semiconductor substrate among one pair of box marks, By being the position doubling mark to which it consisted of a slit of the shape of a frame mostly arranged from the periphery of an opening slot in an equidistant position, and the box mark of another side was formed in opening Mizogami among one pair of box marks Since the layer insulation layer arranged equally [****] is prepared between the opening slot and the slit, when a reflow occurs in the aforementioned layer insulation layer again, configuration change of an edge fraction can obtain as a semiconductor device which comes to have the opening slot suppressed to the minimum extent. Though configuration change of an edge fraction furthermore happens to an opening slot to some extent in this case Since a layer insulation layer is arranged almost equally to the center of an opening slot between an opening slot and an edge fraction by dividing the layer insulation layer by the slit of the shape of a frame mostly arranged from the periphery of an opening slot in an equidistant position, Since configuration change of the edge fraction of an opening slot happens almost corresponding to the distance from the center of an opening slot and the wave of the data in which the position gap measurement result in the edge fraction

of an opening slot is shown turns into the wave corresponding to the distance from the center of an opening slot mostly similarly, The amount of position gaps can be correctly measured from the data in which the aforementioned position gap measurement result is shown. Since the production by the low cost is attained in itself as a result of being able to obtain as a semiconductor device which comes to have a relative-position relation with optimum pattern and design pattern of the following process which preexist on a semiconductor substrate, therefore the product yield's is constituted as a good semiconductor device by the above, it can obtain as a cheap semiconductor device.

[Translation done.]